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DEVELOPMENT OF GaN MOSFETS AND MISFETS

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Technical Report

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SUMMARY

The purpose of this program is to develop GaN power MOSFETs and IGHFETs using novel gate dielectrics. In the past year we have: 1) demonstrated low D_{it} , $1-4 \times 10^{11} \text{ eV}^{-1} \text{ cm}^{-2}$, oxide/GaN interfaces using low temperature deposition of Sc_2O_3 and MgO , 2) investigated the microstructure of the MgO low T dielectric and determined it to be single crystal at the semiconductor interface, 3) demonstrated, for the first time, inversion in a GaN device using a gate-controlled diode and 4) begun development of $\text{MgO}/\text{AlGaIn}/\text{GaN}$ IGFETs. As part of the effort to develop power devices, we have also investigated the effect of our low T dielectrics on the passivation of AlGaIn/GaN power devices in collaboration with WPAFB. Improvements in power performance up to 3 dB have been obtained using MgO to suppress surface leakage.

ACCOMPLISHMENTS

TASK 1) Develop gate dielectrics with improved performance and reproducibility

Scandium Oxide

Sc_2O_3 exists in the same Bixbyite structure as Gd_2O_3 but has a much smaller lattice constant, which should make it less defective when deposited on GaN[1,2]. Like Gd_2O_3 it has a high melting point suggesting good thermal stability.[1] The material is often used as an optical coating for high power photonic devices and has a bandgap of 6.3 eV.[1] Based upon the reported work function of 4eV [1] it is likely that the electron affinity is $\sim 0.85\text{eV}$. If this estimate is correct then, unlike Gd_2O_3 , the band offsets for Sc_2O_3 should allow fabrication of devices on both n- and p-type material. The dielectric constant is also favorable as it is slightly larger than that of Gd_2O_3 , 14 vs. 11.

Similar to the Gd_2O_3 , Sc_2O_3 deposited by GSMBE using elemental Sc and an ECR oxygen plasma also produces extremely smooth surfaces as indicated from AFM and SEM.[3,4] RMS roughnesses of 0.5 to 0.8 nm were seen for substrate temperatures of 100°C or 600°C, respectively. Using AES depth profiling and surface scans, it was shown that the MBE derived Sc_2O_3 was of uniform concentration throughout the film, as shown in Figure 1. The O:Sc ratio, as measured from comparing Auger peak to peak heights, was 0.85 to 0.90 and was not strongly dependent on either substrate or Sc cell temperature. The growth rate of the scandium oxide was 0.67nm/min for $T_{\text{Sc}}=1130^\circ\text{C}$ and 1.25nm/min for $T_{\text{Sc}}=1170^\circ\text{C}$, and again was found to be independent of substrate temperature.

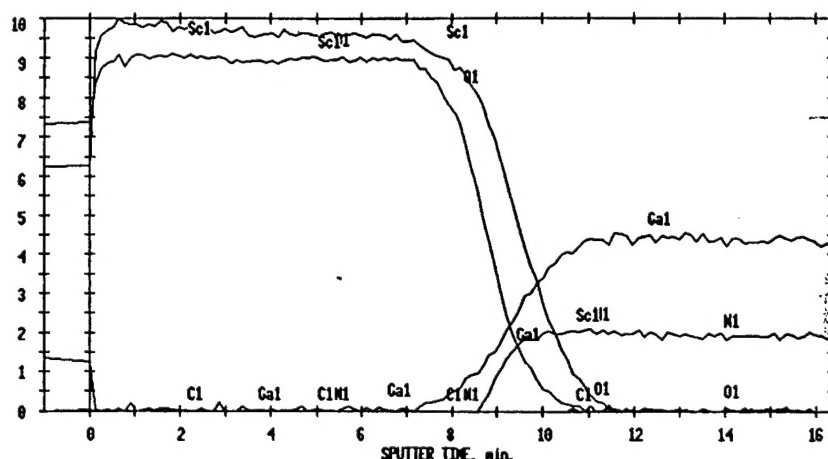


Figure 1. AES depth profile of Sc_2O_3 on GaN. The conditions of the oxide growth were

$$T_{\text{Sc}}=1130^\circ\text{C} \text{ and } T_{\text{sub}}=100^\circ\text{C}.$$

From HXRD results, it was found that for the higher growth temperatures, the scandium oxide (111) plane grew parallel to the surface (0001) GaN as was also seen in the high temperature Gd_2O_3 films grown on GaN.[3] The 20% mismatch between the (111) Gd_2O_3 and the GaN (0001), leads to a highly defective single crystal layer, resulting in a full-width-at-half-maximum (FWHM) of over 800 arcseconds in HXRD scans. The smaller mismatch between the Sc_2O_3 and the GaN (0001) should lead to a lower defect density and in fact the FWHM is substantially reduced at 514 arcseconds as compared to the 883 arcseconds found in the best Gd_2O_3 , shown in Figure 2. From the RHEED data, it appears that reducing the substrate temperature changes the film microstructure from defective single crystal to amorphous or polycrystalline after the first few minutes of growth, just as was the case for the Gd_2O_3 . However, it is not known if the initial Sc_2O_3 material deposited at low temperature is single crystal.

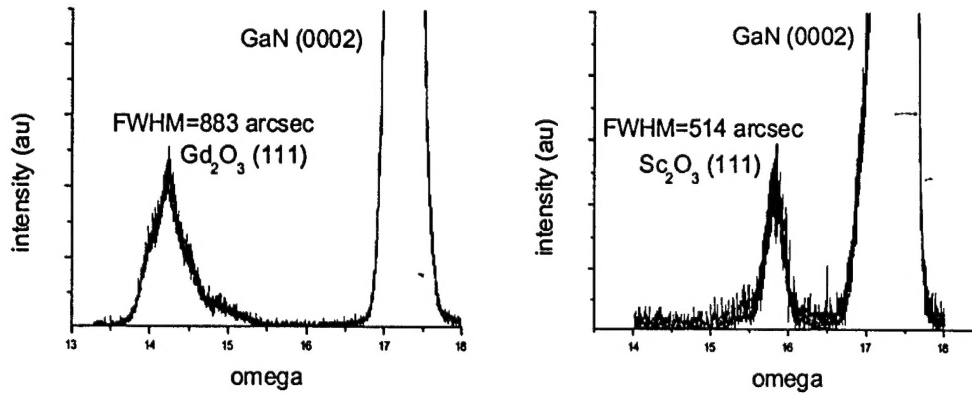


Figure 3. HXRD scans of dielectrics grown at 600°C on GaN: at left, Gd₂O₃, at right, Sc₂O₃.

Diodes fabricated from 40nm of Sc₂O₃ grown on n-GaN at 600°C show a forward breakdown field of only 0.7MV/cm, as shown in Table 1.[4] While this represents an improvement over the Gd₂O₃, the leakage is still so severe that further electrical characterization is not possible without the use of some form of

cap. This leakage can be reduced by annealing at 1000°C in nitrogen, which improves the breakdown field to 1.4MV/cm. However, C-V analysis shows that the anneal severely degrades the interface, producing D_{it} values of $\sim 10^{13} \text{ cm}^{-2} \text{ eV}^{-1}$. As with the Gd₂O₃, low deposition temperatures did improve the breakdown field to $\sim 1.5 \text{ MV/cm}$. The D_{it} for the low temperature material was found using the Terman method to be $\sim 4 \times 10^{11} \text{ eV}^{-1} \text{ cm}^{-2}$ near the conduction band edge, again similar to that observed for Gd₂O₃.

Table 1. Interface state density, D_{it} , calculated using the Terman method, and breakdown field at 5 mA/cm^2 , V_{BD} , for various dielectrics grown on n-GaN by GSMBE using an ECR oxygen plasma.

Dielectric	D_{it} ($\text{eV}^{-1} \text{ cm}^{-2}$)	V_{BD} (MV/cm)
HT-Gd ₂ O ₃	3×10^{11}	0.1
LT-Gd ₂ O ₃	6×10^{11}	3.0
HT-Sc ₂ O ₃	NA	0.7
LT-Sc ₂ O ₃	4×10^{11}	1.5
LT-MgO	4×10^{11}	1.0

While ECR plasmas are expected to produce the lowest ion energies and hence should produce the least amount of damage to the GaN surface, RF plasmas are expected to produce much more intense plasmas in terms of active oxygen species.

Table 2. Forward breakdown field and interface state density calculated using the AC conductance method ($E_c - E_t = 0.7 - 0.8\text{eV}$) for dielectrics deposited at 100°C on n-GaN using either an ECR or an RF plasma.

	ECR		RF	
	D_{it} ($\text{eV}^{-1}\text{cm}^{-2}$)	V_{BD} (MV/cm)	D_{it} ($\text{eV}^{-1}\text{cm}^{-2}$)	V_{BD} (MV/cm)
LT- Sc_2O_3	8×10^{11}	1.5	$9-11 \times 10^{11}$	1.9
LT-MgO	2×10^{11}	1.2	$2-3 \times 10^{11}$	2.3

Using the RF approach at low

deposition temperatures, the amorphous/poly-crystalline Sc_2O_3 shows slightly less leakage as deposited, with a breakdown field of $\sim 1.9\text{ MV/cm}$, as shown in Table 2. C-V analysis showed modulation from accumulation to deep depletion. Deep depletion with no inversion capacitance is typical for wide-gap semiconductor MIS or MOS structures due to the slow generation rate of the minority carrier at room temperature[5,6]. A significant flat band voltage shift was observed, which indicated the existence of fixed charges in the oxide layer. From C-V analysis the interface state density was calculated using the Terman and AC conductance methods[7,8]. The values determined were $5 \times 10^{11} \text{eV}^{-1}\text{cm}^{-2}$ at $E_c - E_t = 0.2\text{eV}$ (Terman) and $8 \times 10^{11} \text{eV}^{-1}\text{cm}^{-2}$ at 0.7eV (AC conductance). Additional AC conductance measurements conducted at 300°C showed an interface state density of $1.11 \times 10^{12} \text{eV}^{-1}\text{cm}^{-2}$ at $E_c - E_t = 0.42\text{eV}$. No information is yet available on the thermal stability of low temperature Sc_2O_3 .

MgO

MgO is a rock salt dielectric which has been explored as an intermediate buffer layer for growth of ferroelectric materials on semiconductors[9,10] or as a potential gate dielectric for GaAs [11,12] or Si.[10] While MgO deposition by MBE has been successfully demonstrated by a number of groups, the crystal quality of the films deposited on GaAs and Si has been poor due to the large lattice mismatch between the MgO and the semiconductor substrate. GaN has a smaller lattice constant than GaAs and is thus a much closer match to MgO. [2,13] An additional advantage of this system is the large bandgap and thus large band offsets that are expected relative to either an n- or p-type semiconductor. Further, the dielectric constant for MgO, 9.8, is substantially higher than for SiO₂.

Because of the high Mg vapor pressure, MgO cannot be grown at the same MBE growth temperatures used for the Bixbyite oxides. Above ~350°C the growth rate drops precipitously with growth temperature.[14] At a substrate temperature of 100°C, the RHEED pattern remains streaky for a few monolayers then changes to a pattern similar to that observed for low temperature growth of Gd₂O₃. At 350°C the same transition is observed, though the final RHEED pattern appears to be more poly-crystalline than at 100°C, and the film seems to be more textured with an apparent [111] axis perpendicular to the substrate. XTEM of the MgO/GaN interface shows evidence of a thin single crystal layer at the interface in agreement with the RHEED, as shown in Figure 3. In some areas this epitaxial region appears to be as thick as 40-50 monolayers, while in other areas it is substantially thinner.

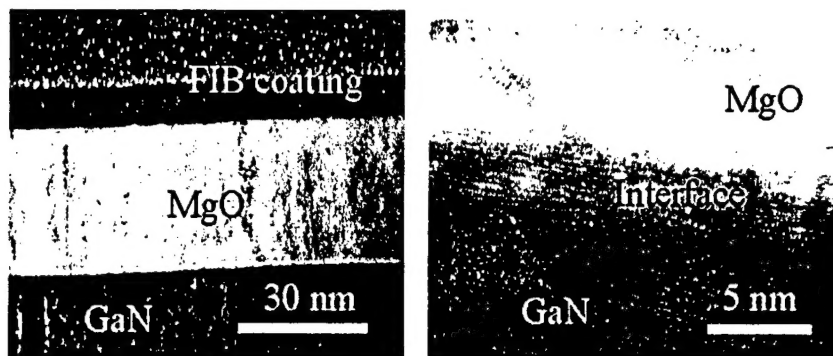


Figure 3. XTEM images of MgO/n-GaN structure grown using an RF oxygen plasma.

Diodes with 100 nm MgO gate dielectrics grown using an ECR plasma show reverse breakdown and forward turn-on voltages of >40 V and >10 V_f (where these parameters are defined as the values at 100 nA and 5 mA/cm², respectively). A forward breakdown field of 1.2 MV/cm for the MgO was calculated from this data. The measured C-V curve at a frequency of 1 MHz and sweep-rate of 100 mV/s showed a clear deep depletion behavior for negative bias voltage and no measurable hysteresis was observed. The interface state density was calculated using the Terman method to be $4 \times 10^{11} \text{ eV}^{-1} \text{ cm}^{-2}$ at 0.3 eV below the conduction band edge. The conductance technique was also used to characterize the MgO/GaN MOS capacitors, and an interface state density of $2 \times 10^{11} / \text{eV} \cdot \text{cm}^2$ at $E_c - E_t = 0.7$ eV was obtained. The AC conductance technique is not able to measure interface traps with a time constant much longer than the period of the applied AC signal, because these traps cannot respond to the AC perturbation. Therefore, high temperature AC conductance analysis was carried out over a temperature range of 25 to 300 °C to investigate the traps with longer time constants. Using this approach, the interface trap density was found to increase linearly from room temperature to 200 °C and begin to level off at 300 °C, as shown in Figure 4. The interface trap density was almost three times larger at 300 °C as compared to that at room temperature. This may have significant impact on the MOSFET

performance at elevated temperatures. In general, however, the performance of the MgO dielectric appears to be superior to that of the Bixbyite oxides. This is most likely due to the reduced mismatch between the MgO and the GaN relative to the other oxides and to the larger bandgap of this material.

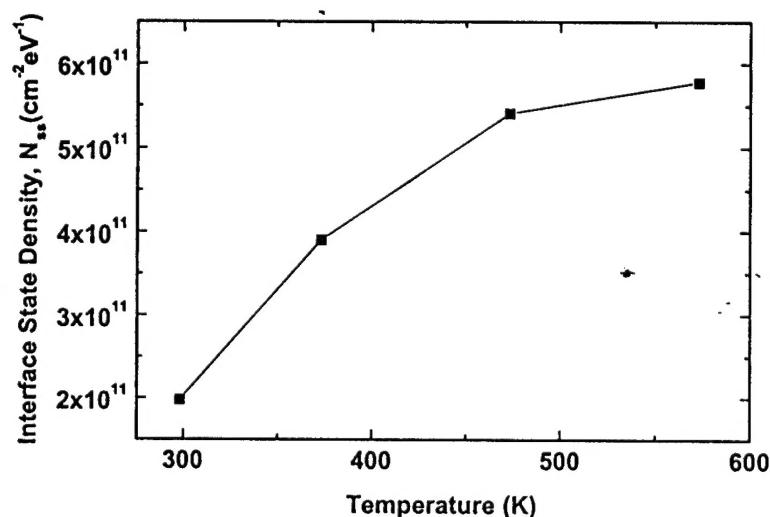


Figure 4. The interface trap density in an ECR grown MgO/n-GaN diode measured at different temperatures using the AC conductance method.

As with the Sc_2O_3 , both ECR and RF plasmas have been explored for the growth of MgO dielectrics. In the case of the MgO, the RF appears to produce substantial improvement in both morphology, as shown in Figure 5, and in the breakdown field, as shown in Table 2. The interface state density is only slightly higher with the RF-grown material, suggesting that ion damage from the RF is not occurring. The higher breakdown field is probably related to the improved morphology. The reason for the improvement in morphology is still under investigation, however it most likely stems from a higher concentration of active oxygen species at the growth surface.

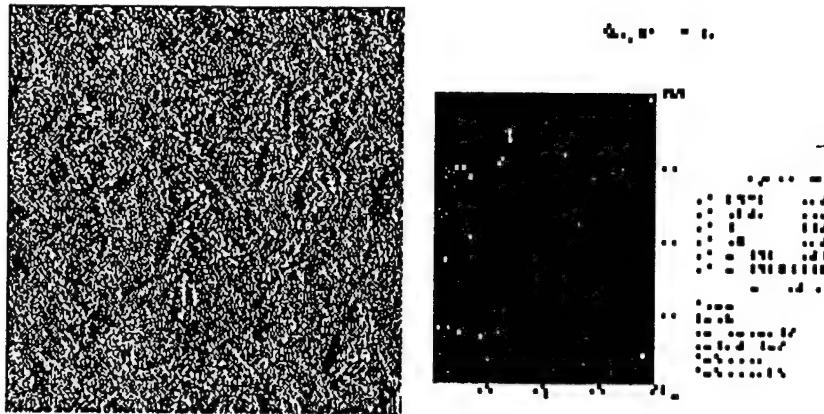


Figure 5. AFM images of MgO grown on n-GaN using ECR (at left) or RF (at right) oxygen plasma sources. The scale is 10 μ m.

TASK 2) Fabricate Enhancement mode GaN MOSFET devices

Realization of an enhancement mode GaN device requires the ability to create inversion in the channel. However, a clear demonstration of surface inversion has proven elusive in GaN due to the very low minority carrier generation rate in GaN at room temperature. Even at 300°C in conventional GaN MOS devices, the generation rate is still too low to observe inversion. To overcome a similar problem in SiC MOS devices, the n^+p junction of a MOS gate-controlled device was employed as an external source of inversion charge[15]. A similar approach has been used to observe inversion in MgO/p-GaN gate-controlled MOS diodes in which n^+ gated contact regions were created by Si^+ implantation and subsequent activation annealing with the MgO gate oxide in place. The MgO was deposited by MBE at 100°C on a p-GaN($p \sim 3 \times 10^{17} \text{cm}^{-3}$ at 25°C) layer grown by metal organic chemical vapor deposition on sapphire. The MgO was grown using elemental Mg and RF plasma-activated oxygen to a thickness of $\sim 80 \text{nm}$. For diode fabrication, implantation of 70, 195, 380 keV $^{29}Si^+$ ions at a dose of 2×10^{13} , 6×10^{13} , $1.8 \times 10^{14} \text{cm}^{-2}$, followed by high temperature($\sim 950^\circ\text{C}$) activation annealing, was used to create the n^+ gate-

contact regions. The reverse breakdown of the diode with as-deposited dielectric was $\sim 12\text{V}$, with a forward turn-on voltage of $\sim 10\text{V}$. Figure 6 shows C-V characteristics of the MgO/GaN MOS-controlled diodes at 25°C in the dark as a function of the measurement frequency. In each case, -20V was applied at the gated contact to provide a source of minority carriers. The frequency dispersion observed in inversion is due to the resistance of the inversion channel, as reported for n^+p SiC MOS gate-controlled diodes.[15] At 5KHz measurement frequency, only deep depletion is seen since the characteristics are dominated by majority carriers[16]. As the frequency is decreased, a clear inversion behavior is observed due to charge flow into and from the n^+ regions external to the gate. Figure 6 also shows I-V characteristics from the diodes at 25°C in the dark. For the accumulation region at negative bias, the reverse current is mainly due to diffusion and generation in the depletion region. As the bias is moved to positive values, the current increases due to the presence of two additional components, namely the additional depletion region under the gate provides more gate current and the surface generation current increases. As the bias is further increased to the inversion region, this surface generation component is suppressed, leaving only current due to generation in the depletion region. This is the classical behavior for a gate-controlled diode[17]. In light of this result the prospect for realization of enhancement-mode GaN MOS transistors appears to be quite good.

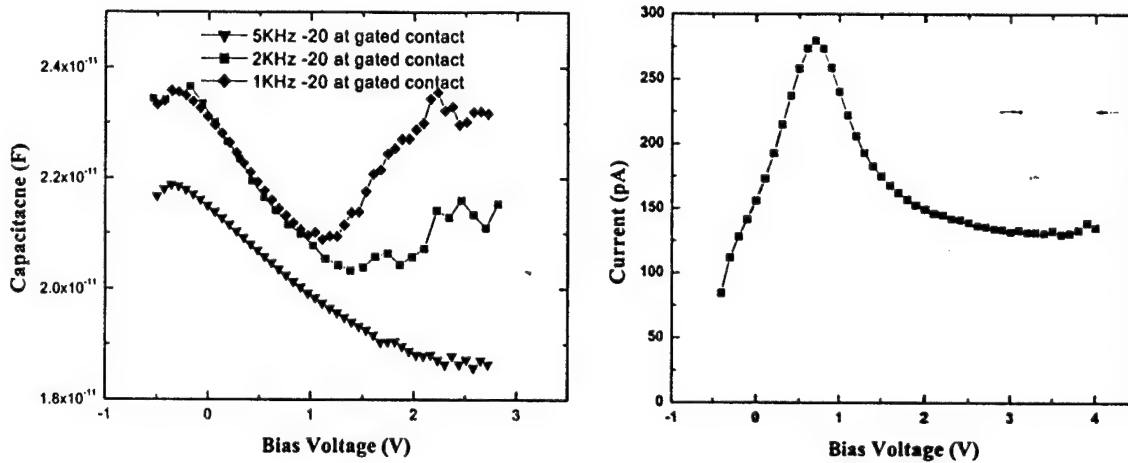


Figure 6. C-V and I-V characteristics of MgO/n-GaN gate controlled diode.

TASK 3) Fabricate Insulated Gate Heterostructure Field Effect Transistors (IG-HFETs)

We have begun developing the oxide deposition and processing steps necessary for fabrication of IG-HFETs using the dielectrics discussed in previous sections. Two areas are currently being addressed. Firstly the type of cap on the HFET base structure must be optimized. Initial results suggest that GaN caps may prove most amenable to oxide deposition as the AlGaIn caps are more difficult to clean and may lead to enhanced interface state densities. Secondly, the need to alloy the Ohmic contacts makes it necessary for the oxide to undergo a severe thermal anneal after deposition. We are presently studying the thermal stability of the MgO and Sc₂O₃ dielectrics. The information generated from this study will be used to develop a process sequence for the IGHFET which does not compromise the gate dielectric.

TASK 4) Fabricate high power GaN Devices

A commonly observed problem in AlGaIn/GaN high electron mobility transistors (HEMTs) is manifested by the observation of current degradation and dispersions in

transconductance and output resistance[18-31]. These phenomena result from the presence of either surface states in the gate-drain region or trap states in the buffer layer of the HEMT structure. With improved control of epitaxial growth purity and stoichiometry in recent years, the surface states appear to present the biggest obstacle to the wide-spread use of AlGaN/GaN HEMTs in high microwave power applications. The use of SiN_x passivation layers on the rf output power and power-added efficiency, and on breakdown voltage and other dc parameters, has been reported in a number of publications[[18-20], [23], [26-30]. It is generally found that the drain-source current and transconductance are increased, along with the output power. In addition, there is a strong reduction of current collapse in structures where buffer trapping effects are small compared to surface trapping of carriers. In collaboration with WPAFB, we have begun investigating the effect of the dielectrics discussed in previous sections on the problem of current collapse. We have found that thin, low temperature layers of Sc₂O₃ and MgO deposited by plasma-assisted Molecular Beam Epitaxy can also effectively mitigate the collapse in drain current through passivation of the surface, and improve the power performance significantly.

The HEMT structures were grown on Al₂O₃ by metal organic chemical vapor deposition. A 3μm thick, undoped GaN buffer was followed by a 30Å thick, undoped Al_{0.3}Ga_{0.7}N spacer, a 220Å thick, Si-doped ($n \sim 5 \times 10^{18} \text{cm}^{-3}$) Al_{0.3}Ga_{0.7}N donor layer and a 50Å thick, undoped Al_{0.3}Ga_{0.7}N cap layer. Device isolation was performed by Cl₂/Ar Inductively Coupled Plasma mesa etching. The e-beam evaporated Ni(200Å)/Au(2000Å) gate metallization was also patterned by lift-off. The dc and large signal characteristics were measured both before and after passivation.

For comparison, 170nm thick SiNx passivation layers were deposited on completed devices using plasma-enhanced chemical vapor deposition in a Unaxis 790 system. The deposition was performed with 13.56MHz rf power at 40W, pressure of 800mTorr with 200 sccm Nitrogen, 600 sccm He, 4 sccm NH₄, and 167 sccm of 3% Silane in Helium, with a deposition temperature of 300° C. The 100Å thick Sc₂O₃ or MgO layers were deposited at 100°C using rf plasma-assisted MBE. Oxygen was supplied from a 13.56 MHz source operating at 300W forward power and 2.5×10^{-5} Torr pressure. Effusion cells operating at 1150°C for Sc or 380°C for Mg provided the metal flux. Prior to oxide deposition, the surface was cleaned ex-situ by exposure to UV/O₃ and in-situ heating to 300°C.

Maps of the saturated drain-source current, I_{DSS} , are shown in Figure 7 for devices either with or without Sc₂O₃ passivation. The average I_{DSS} increased slightly upon deposition of the Sc₂O₃ from 366mA/mm in unpassivated devices to 388mA/mm after Sc₂O₃ deposition. Comparable increases were observed with both SiNx and MgO passivation. As reported previously, this is consistent with passivation of surface states which leads to a decrease in surface depletion[18]. The SiNx produced ~70-75% recovery of the drain-source current during gate lag measurement, while the Sc₂O₃ and MgO were more effective in reducing current dispersion, with 85% and 94% recovery, respectively.

Typical load-pull data for HEMTs before and after SiNx passivation are shown in Figure 8 for a measurement frequency of 4GHz. In all cases, the drain voltage, V_D , was held at 10V, while the gate voltage V_G was -2V. The wafer measurements employed mechanical tuners for matching and there was no harmonic termination under class A operation. The devices were matched for the power testing prior to passivation and were tested under these same conditions

after SiN_x deposition. The difference in output power before and after SiN_x passivation is also shown in Figure 8 and is $< 2\text{dB}$ in all cases.

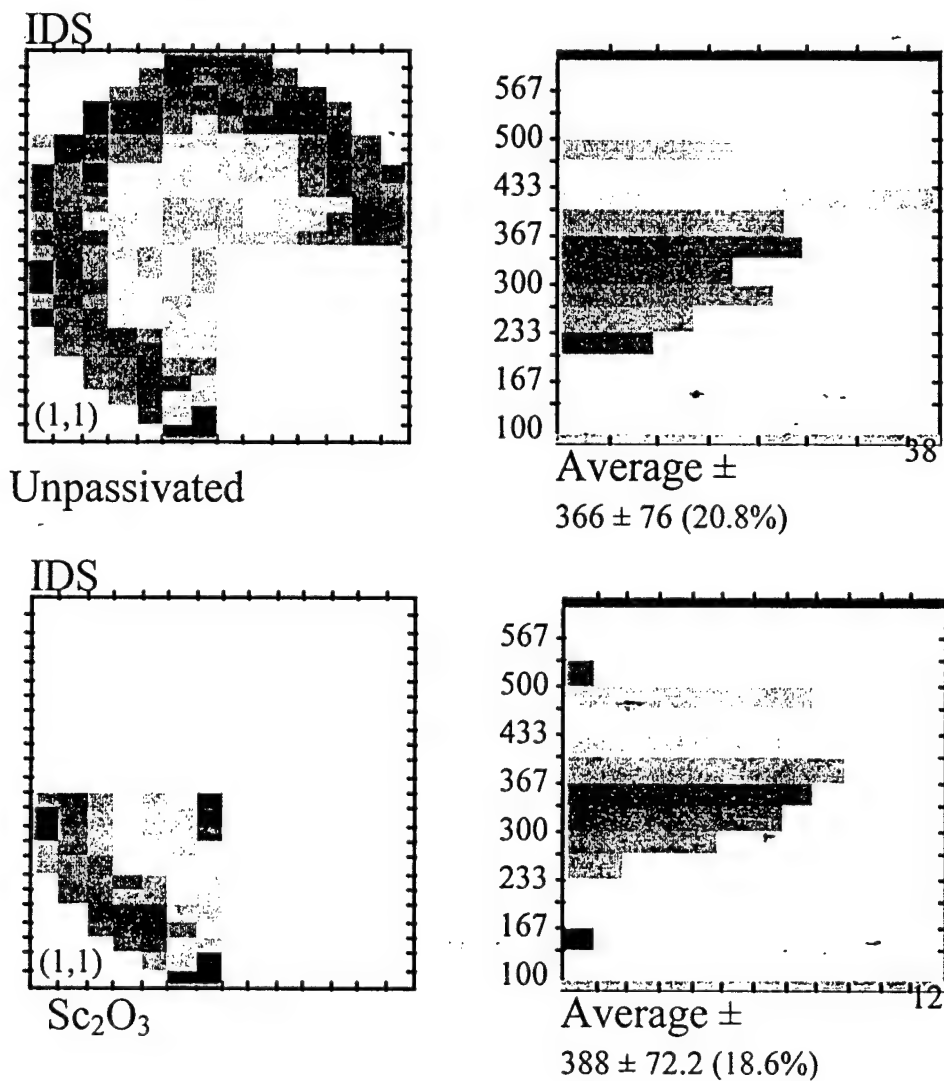


Figure 7. Wafer-map measurements of I_{DSS} for $0.5 \times 100 \mu\text{m}^2$ HEMTs with and without Sc_2O_3 passivation. The data is shown in histogram form at right.

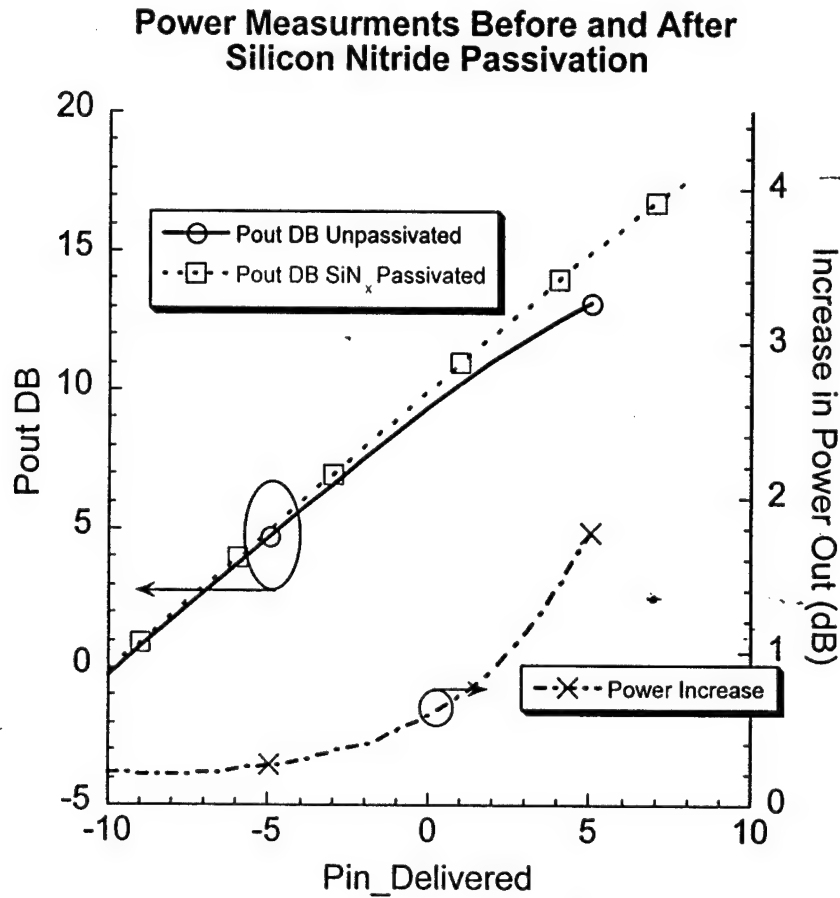


Figure 8. Output power characteristics before and after SiN_x passivation of $0.5 \times 100 \mu\text{m}^2$ devices measured at 4GHz and a bias point of $V_D = 10\text{V}$, $V_G = -2\text{V}$.

Similar data for HEMTs before and after Sc₂O₃ passivation are shown in Figure 9. Note the increased power output compared to typical SiN_x-passivated devices. This is consistent with the higher percentage recovery of I_{DS} during the gate lag measurements with Sc₂O₃ passivation. We believe that the Sc₂O₃ process can be better optimized with respect to the pre-deposition cleaning procedure. The SiN_x deposition has the advantage of a high flux of atomic hydrogen radicals that have proven effective in surface cleaning of other III-V compounds and which can remove native oxide and surface hydrocarbons through formation of volatile reaction products.

The Sc_2O_3 passivation has shown excellent aging characteristics when measured under dc test conditions, with no change in HEMT performance over a period of > 5 months.

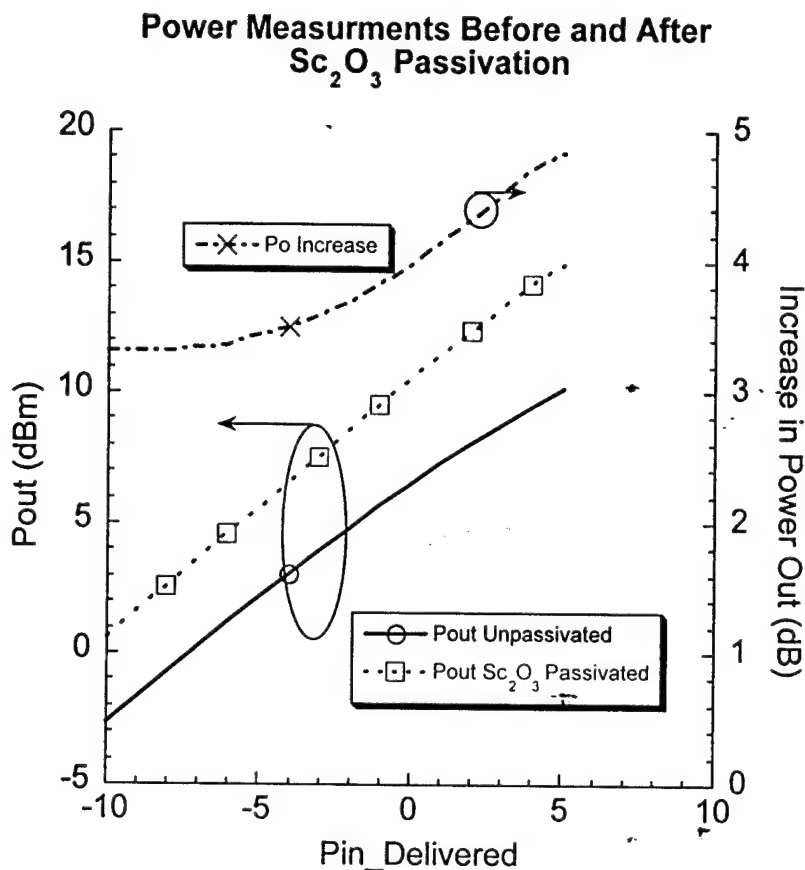


Figure 9. Output power characteristics before and after Sc_2O_3 passivation of $0.5 \times 100 \mu\text{m}^2$ devices measured at 4GHz and a bias point of $V_D = 10\text{V}$, $V_G = -2\text{V}$.

The power measurement data for unpassivated and MgO deposited devices is shown in Figure 10. The output power increases are again significantly larger than for SiN_x passivation of similar devices and the gain remained linear over a wider input power range. A drawback with MgO passivation is that we have observed deterioration of the MgO over a period of months if left uncapped. The MgO reacts with water vapor in the ambient to form MgOH species and we observe increases in interface state densities in MgO/GaN diodes on which the metal is deposited

after a long storage period. By contrast, these changes are not observed in diodes that are immediately metallized after MgO deposition. For the case of using MgO as a passivation layer, we expect it will be necessary to provide an additional encapsulation layer to preserve MgO stability. Since both Sc_2O_3 and MgO are also promising as gate dielectrics for GaN-based devices, one can envision AlGaIn/GaN MISFETs that employ these oxides both for gate oxides and for surface passivation. Hu et. al. have used SiN_x in a similar role in GaN-based HFETs[30].

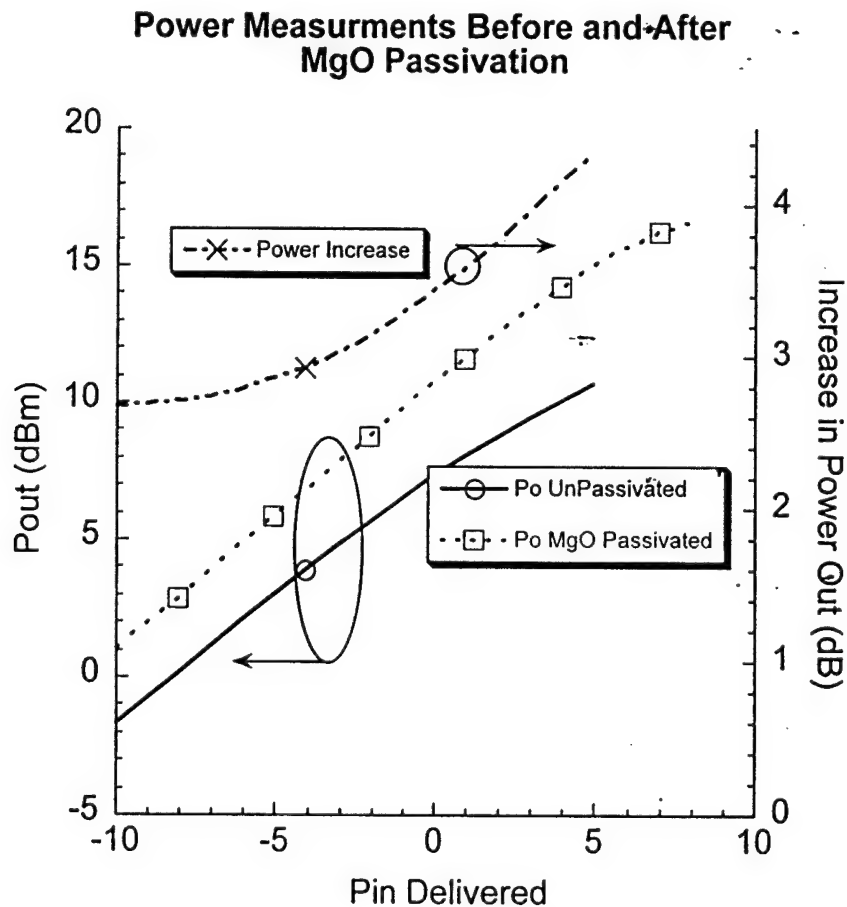


Figure 10. Output power characteristics before and after MgO passivation of $0.5 \times 100 \mu\text{m}^2$ devices measured at 4GHz and a bias point of $V_D = 10\text{V}$, $V_G = -2\text{V}$.

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